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Fig.1A
 (Prior Art)

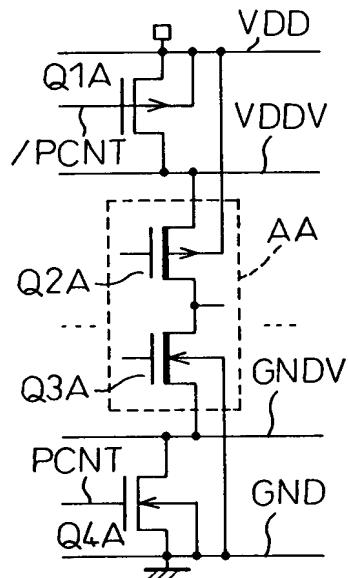


Fig.1B
 (Prior Art)

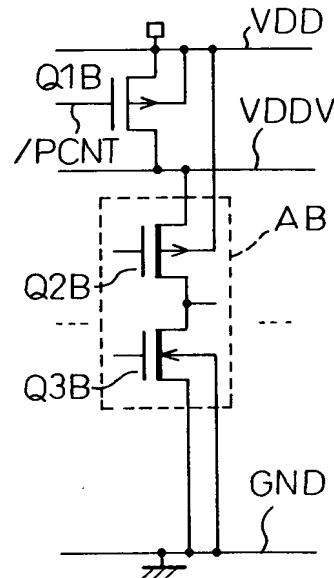


Fig.1C
 (Prior Art)

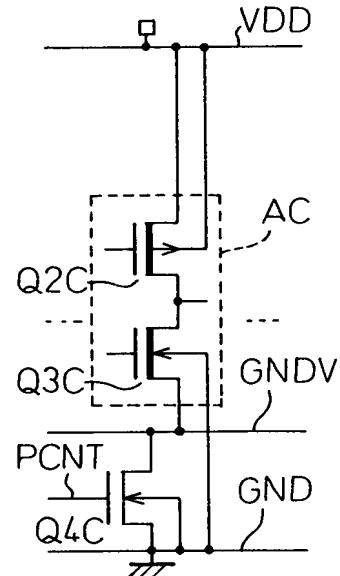


Fig.1D
 (Prior Art)

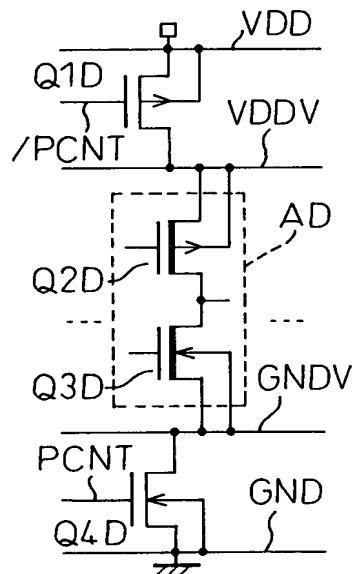


Fig.1E
 (Prior Art)

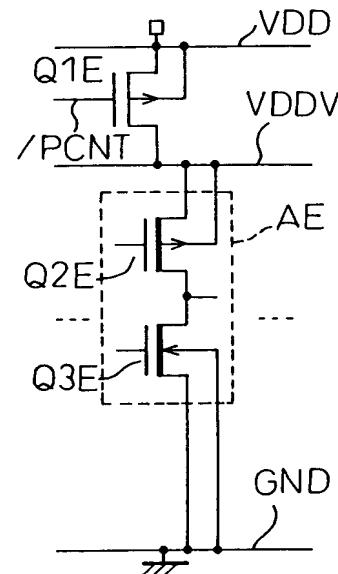
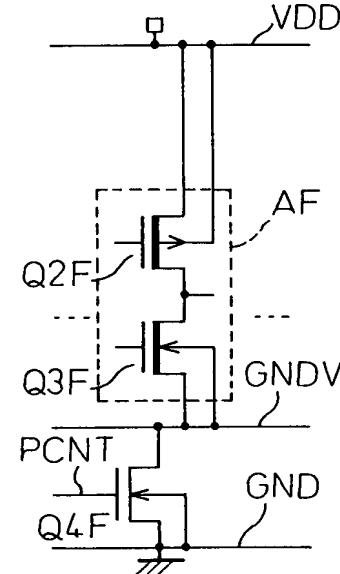


Fig.1F
 (Prior Art)



→ E High-V_{th} NMOSFET

→ E Low-V_{th} NMOSFET

→ E Low-V_{th} PMOSFET

→ E High-V_{th} PMOSFET

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Fig. 2A

(Prior Art)

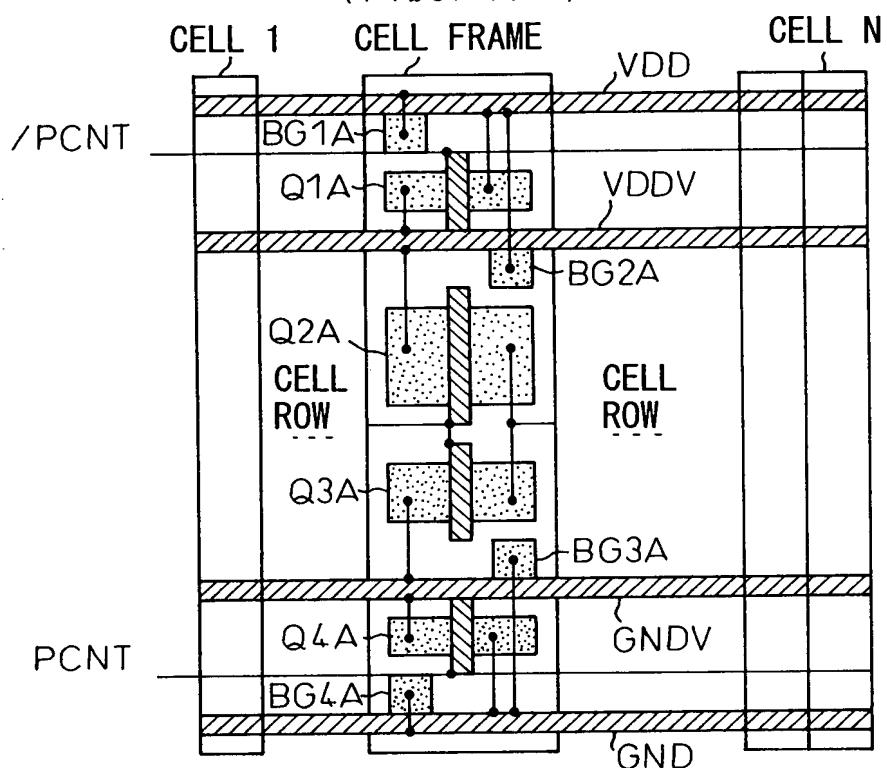
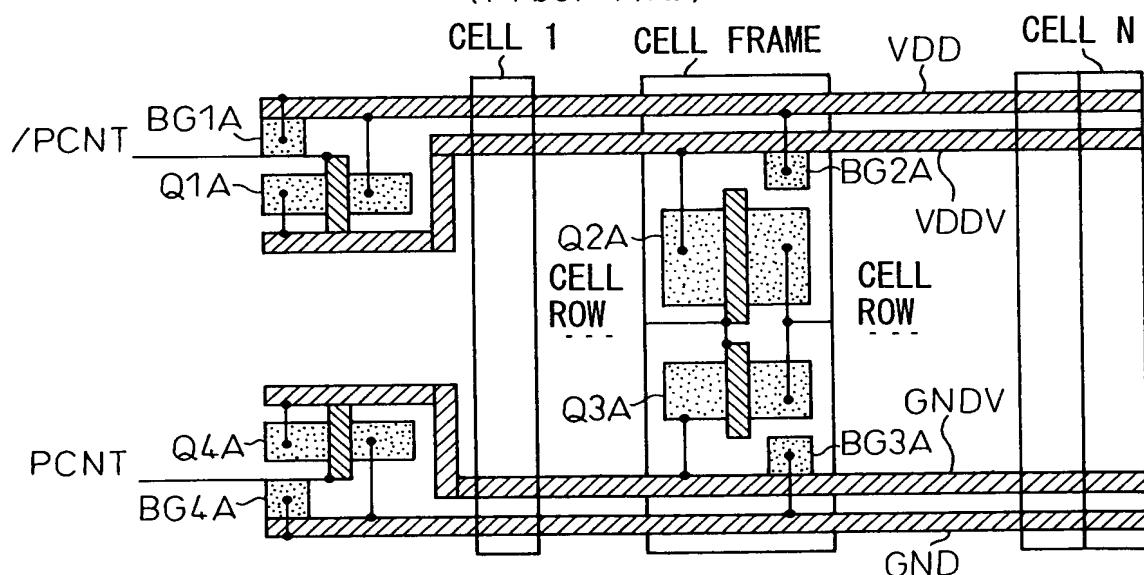


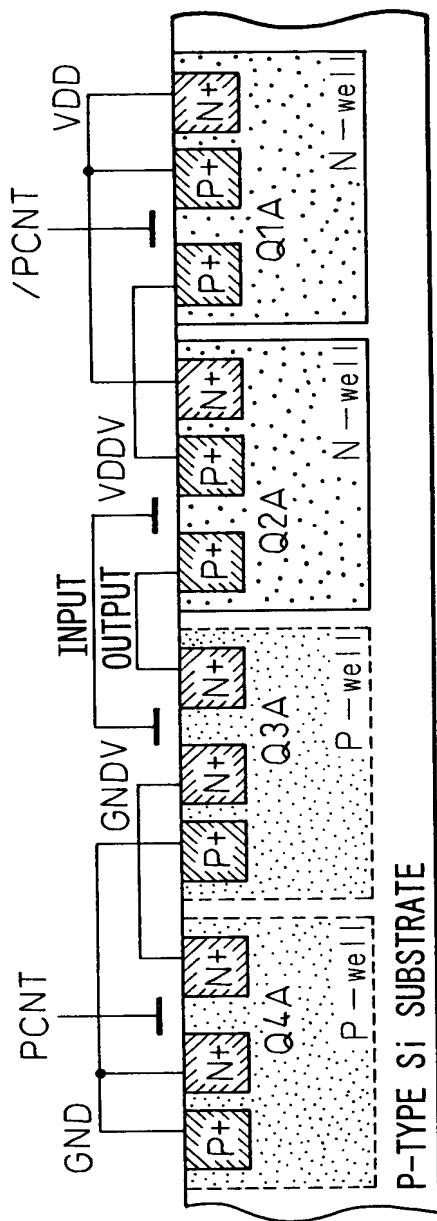
Fig. 2B

(Prior Art)



※ → INDICATES WIRING LINES
AND THEIR CONNECTIONS

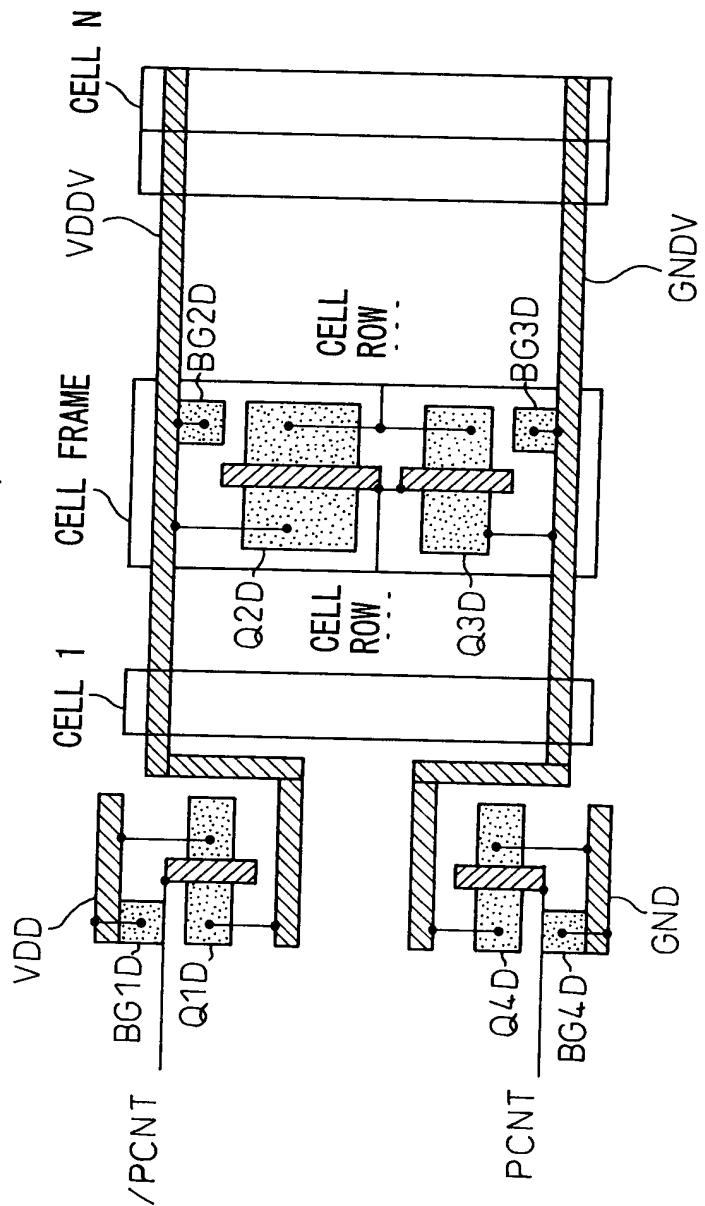
Fig. 3
(Prior Art)

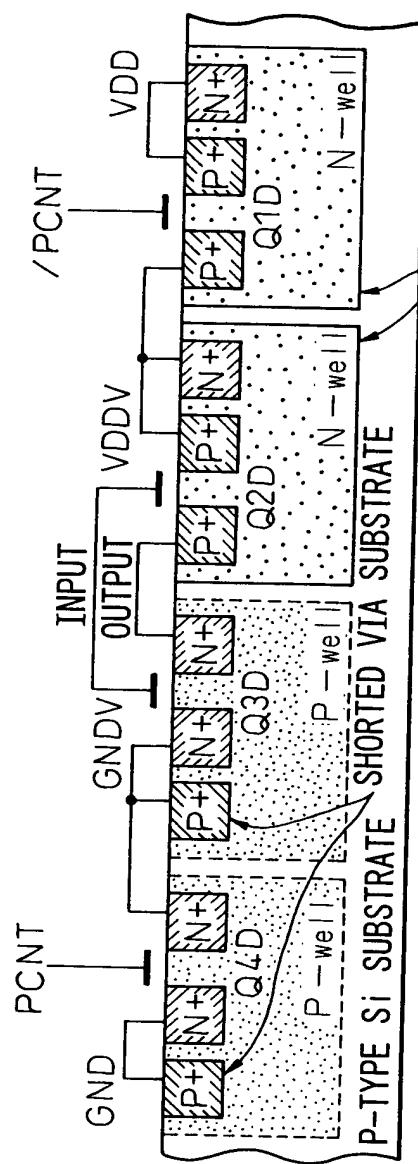


[TWIN-WELL STRUCTURE]

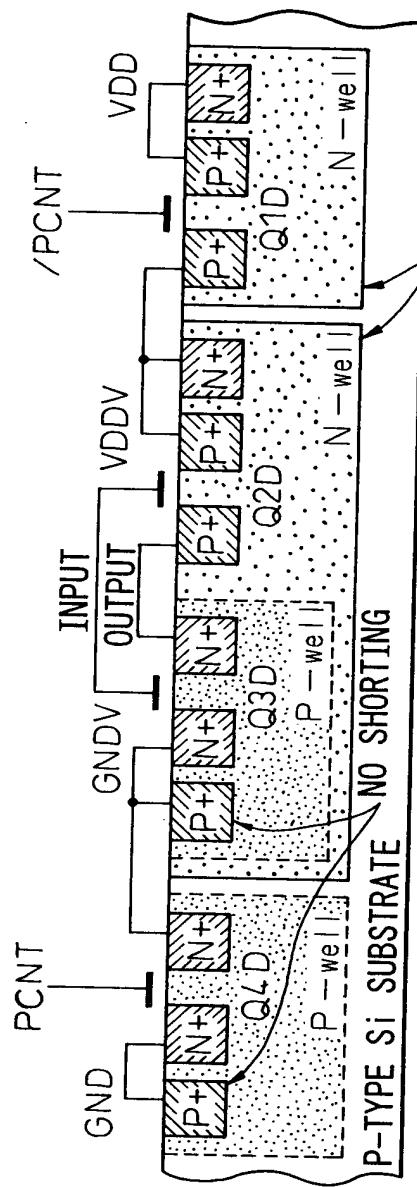
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Fig. 4
(Prior Art)





[TWIN-WELL STRUCTURE] WELLS CAN BE ISOLATED



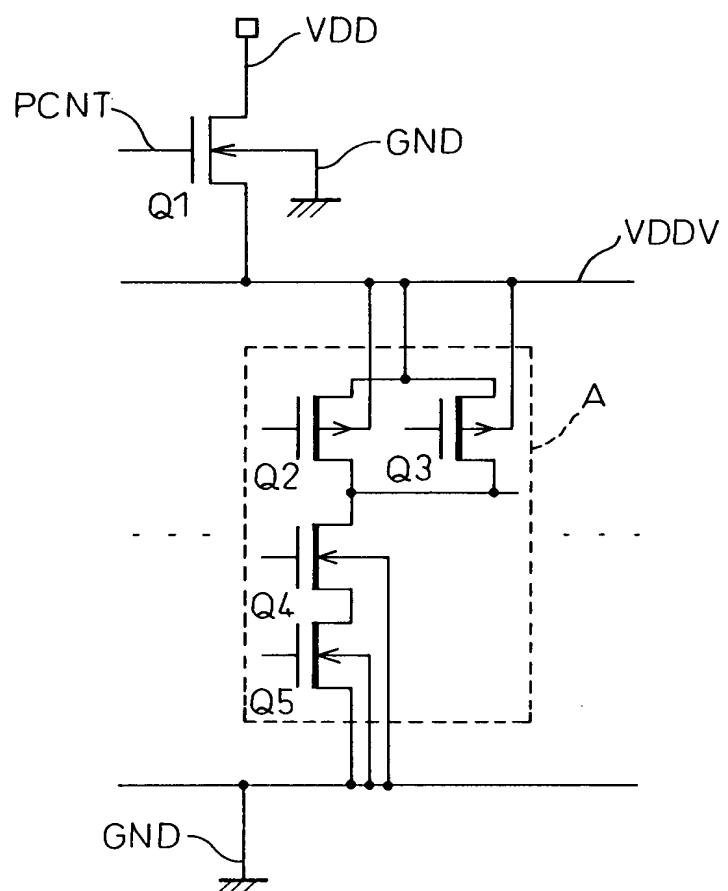
[TRIPLE-WELL STRUCTURE] WELLS CAN BE ISOLATED

Fig. 5A
 (Prior Art)

Fig. 5B
 (Prior Art)

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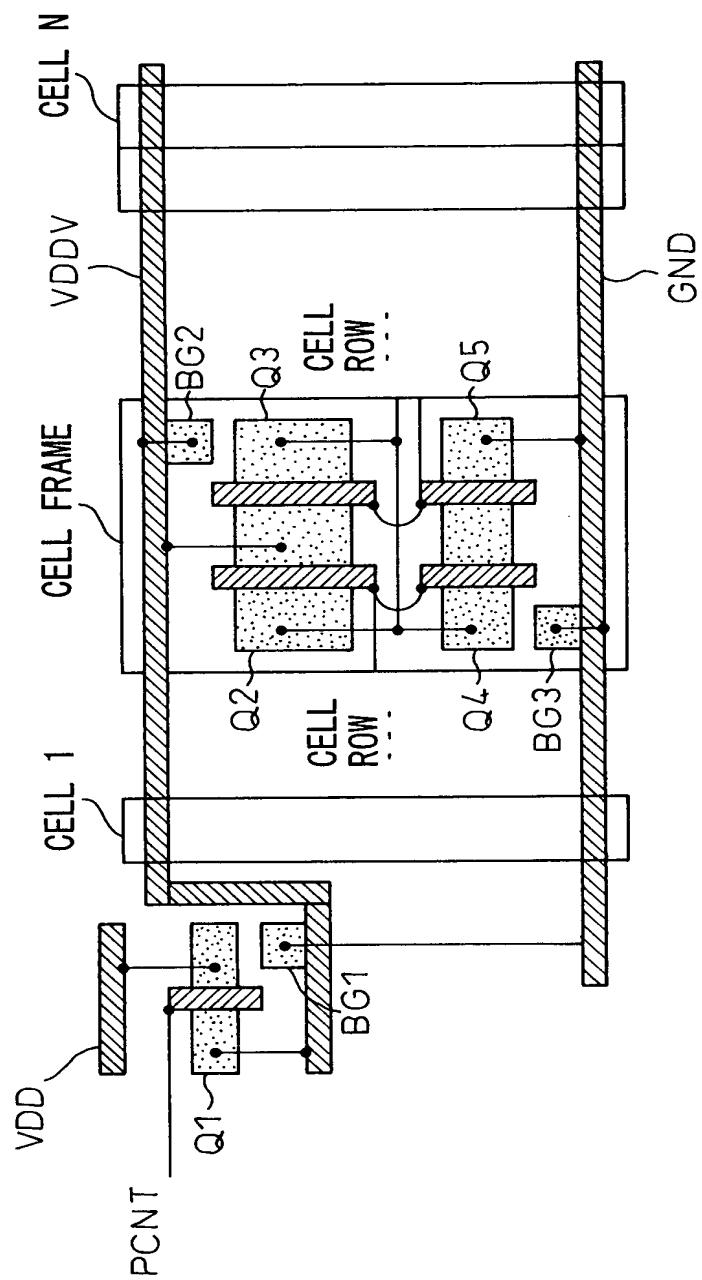
Fig.6



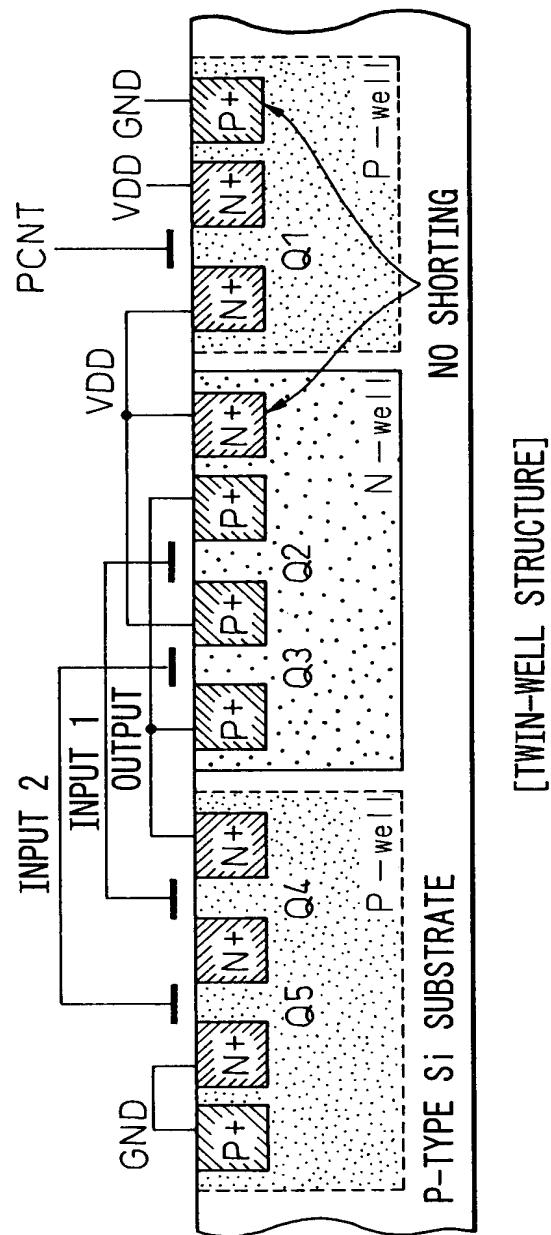
→ ↘ High-V_{th} NMOSFET → ↗ Low-V_{th} PMOSFET
→ ↘ Low-V_{th} NMOSFET

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Fig. 7



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Fig. 9C

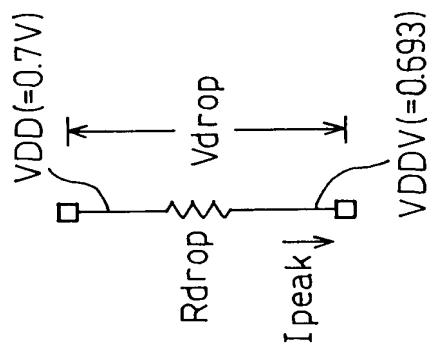


Fig. 9B

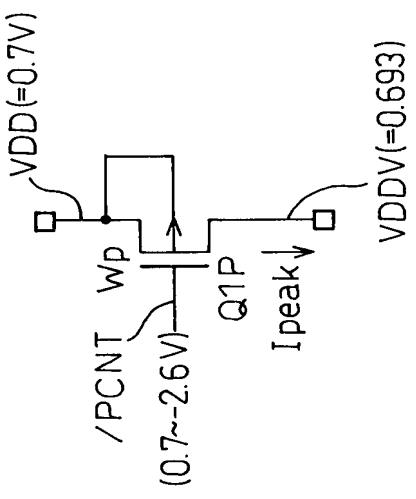


Fig. 9A

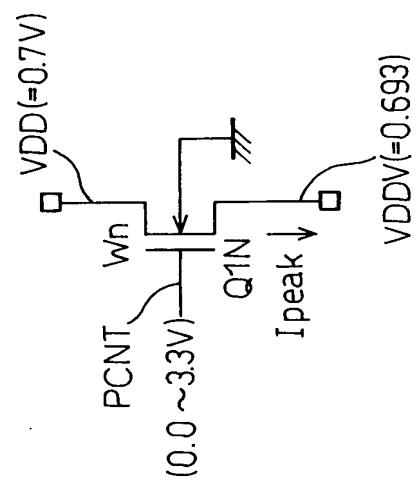


Fig. 10

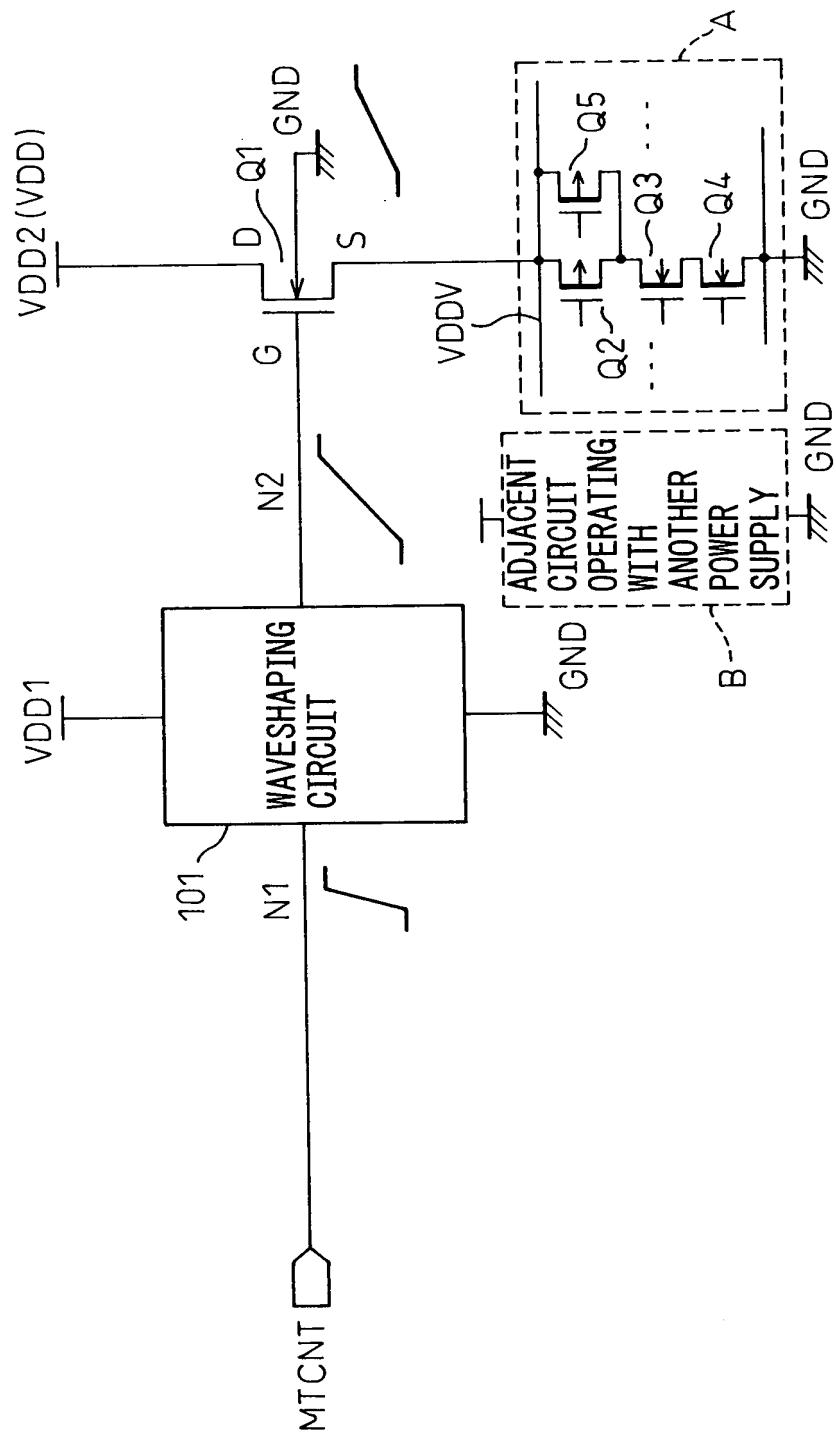


Fig. 11A

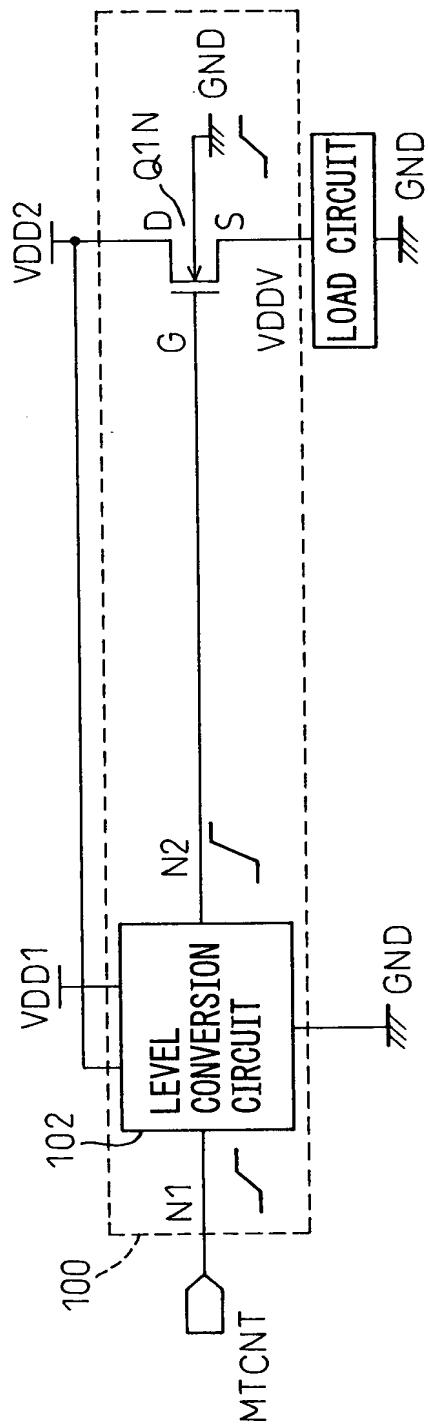
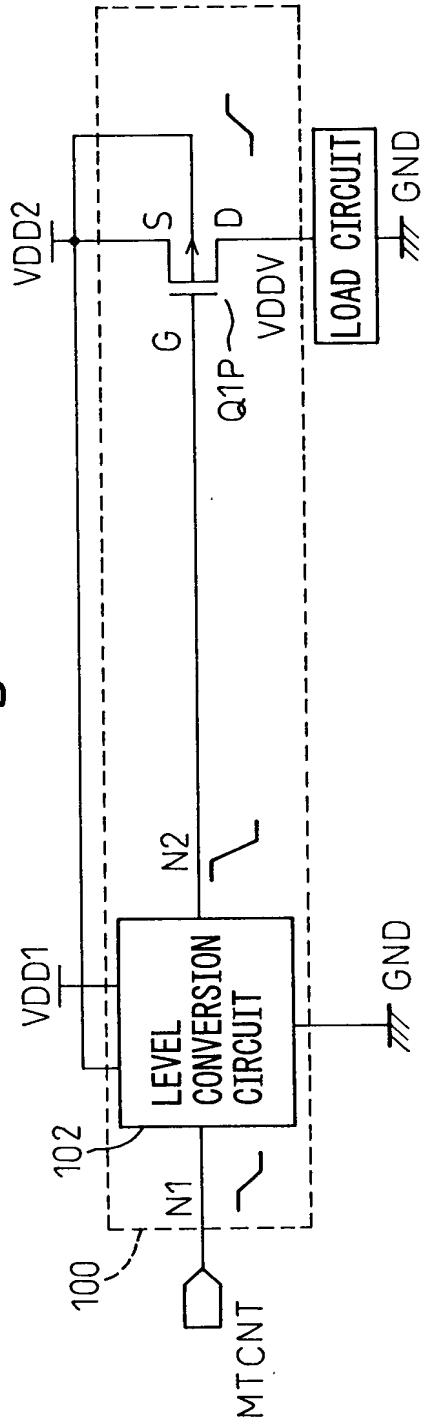
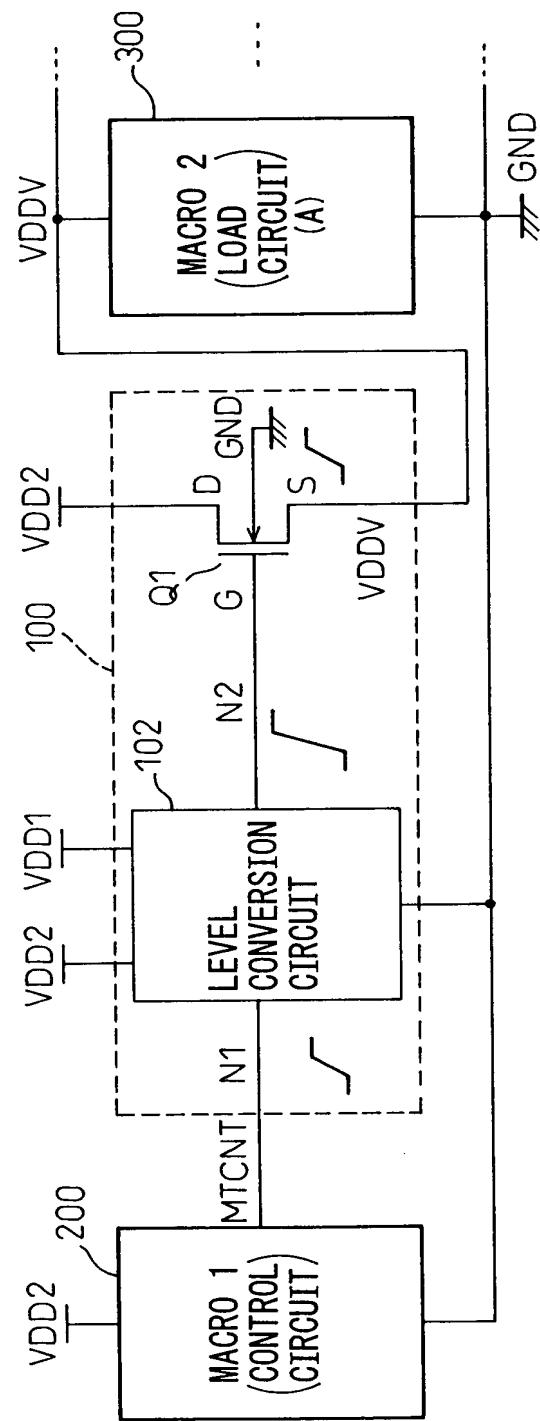


Fig. 11B



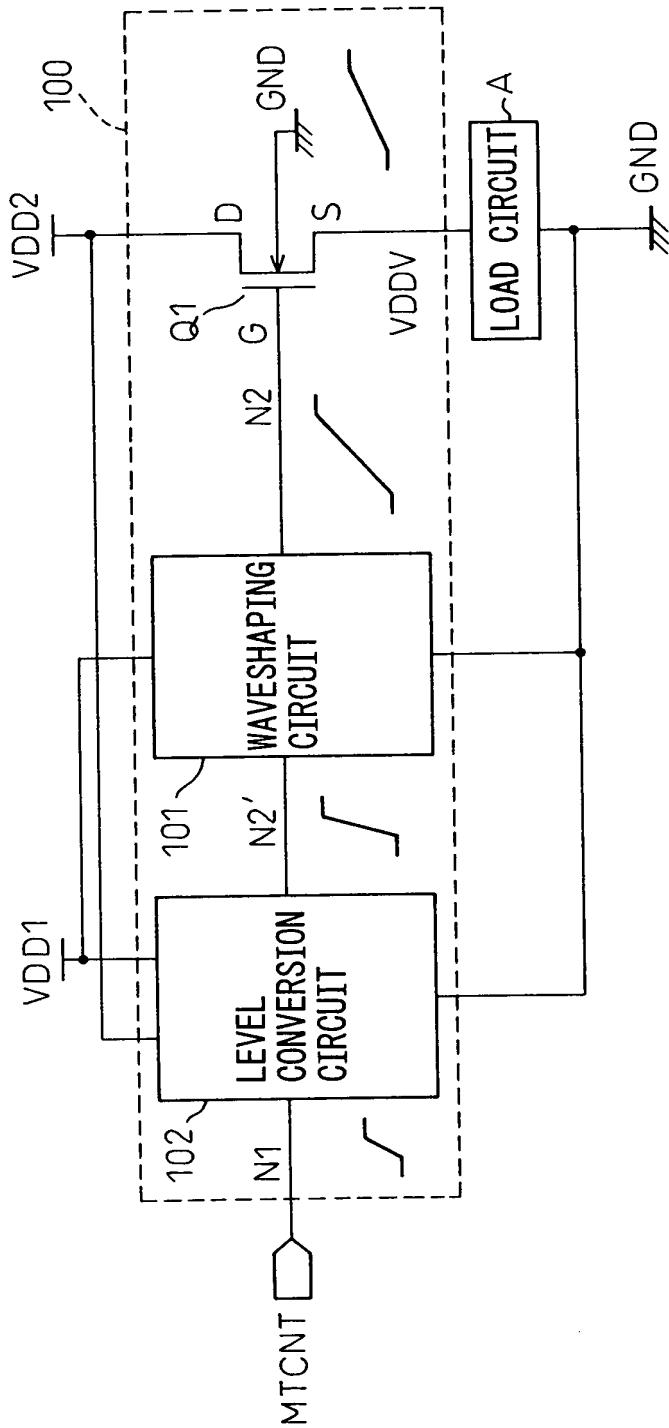
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Fig. 12



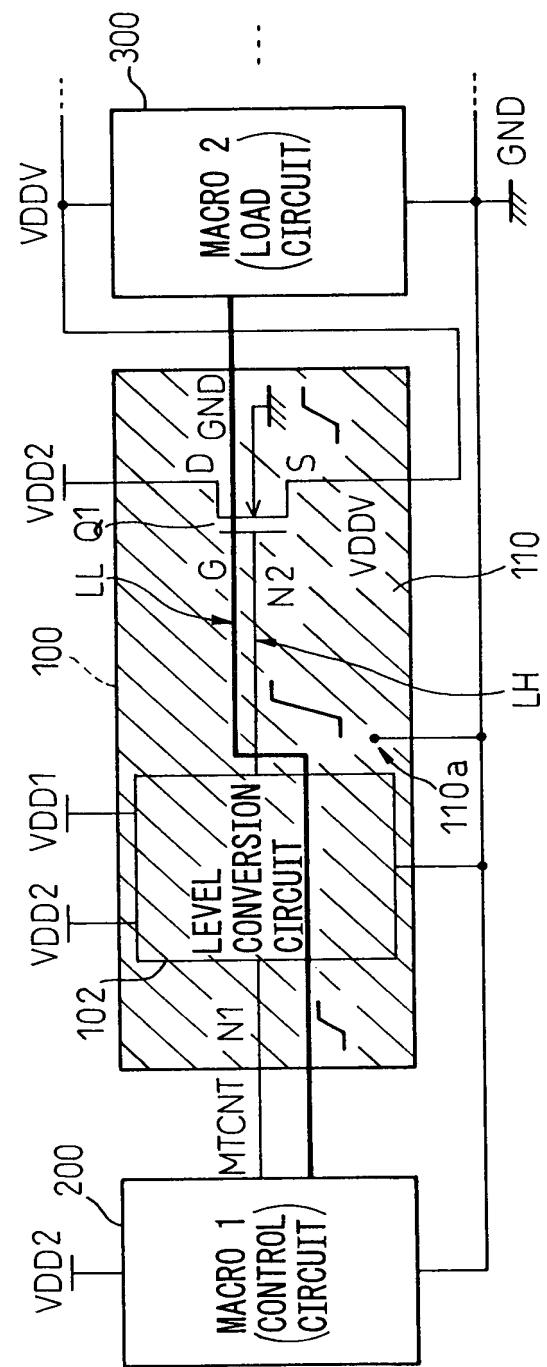
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Fig.13



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Fig. 14



Title: SEMICONDUCTOR INTEGRATED CIRCUIT
DEVICE HAVING A LEAKAGE CURRENT CUTOFF
CIRCUIT, CONSTRUCTED USING MT-CMOS, FOR
REDUCING STANDBY LEAKAGE CURRENT
Inventor's Name: MIYAGI
Application No.: NEW
Docket No.: 100021-00133

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Fig.15

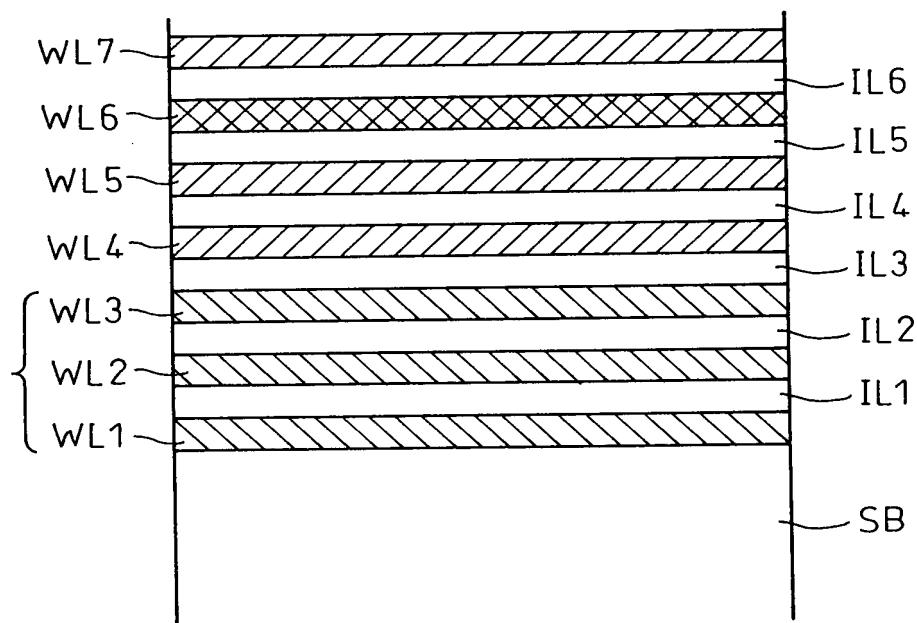
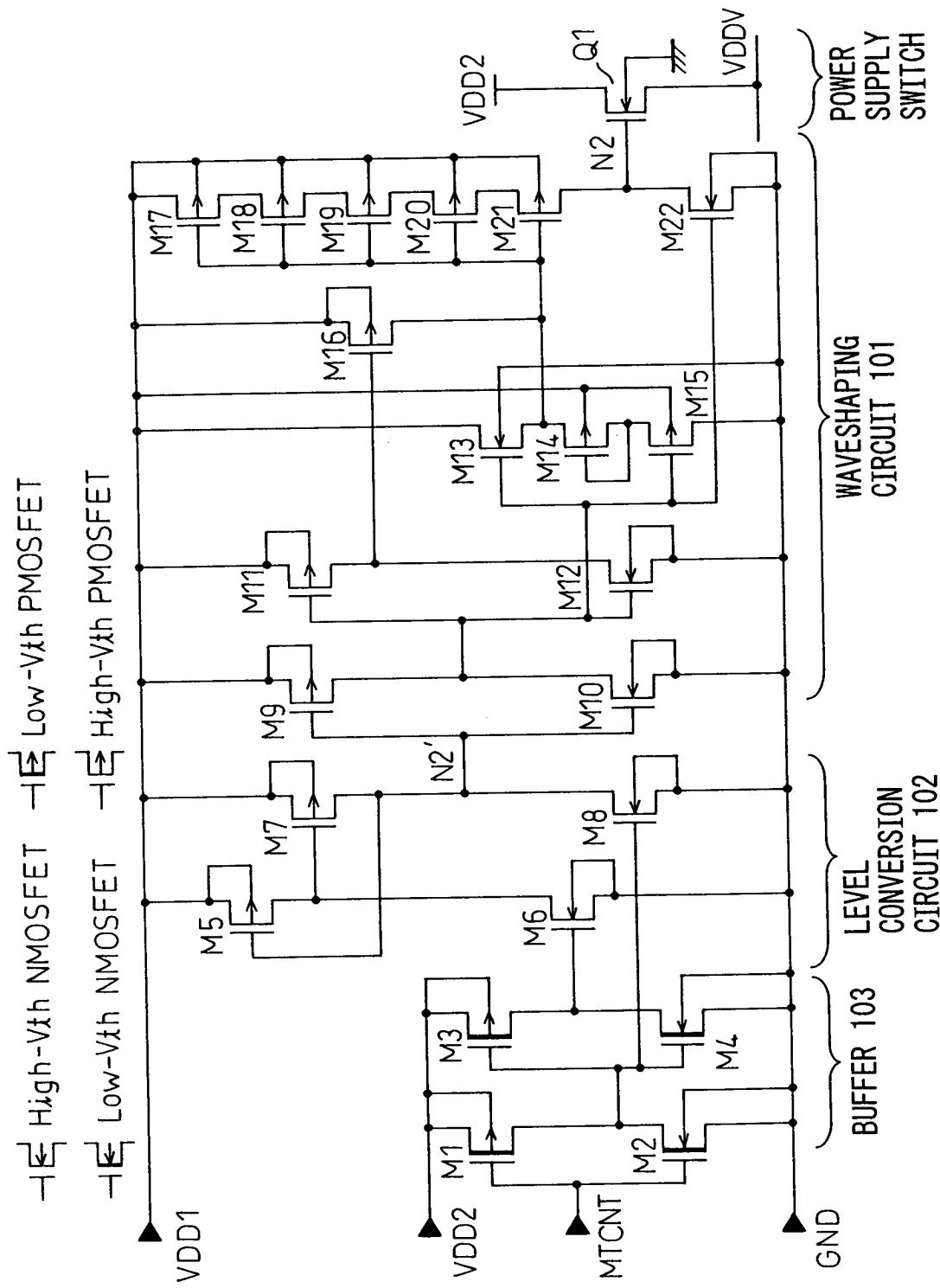


Fig. 16

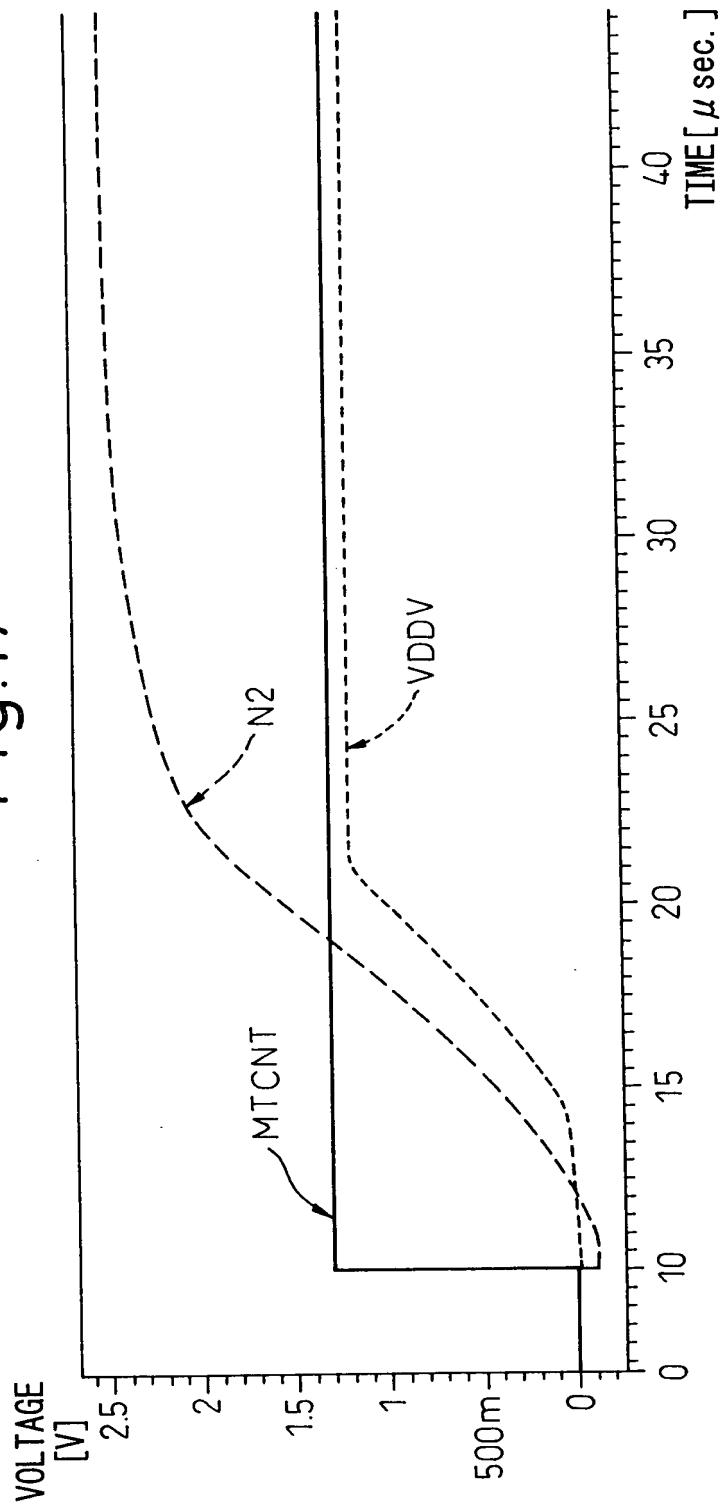


Title: SEMICONDUCTOR INTEGRATED CIRCUIT
DEVICE HAVING A LEAKAGE CURRENT CUTOFF
CIRCUIT, CONSTRUCTED USING MT-CMOS, FOR
REDUCING STANDBY LEAKAGE CURRENT

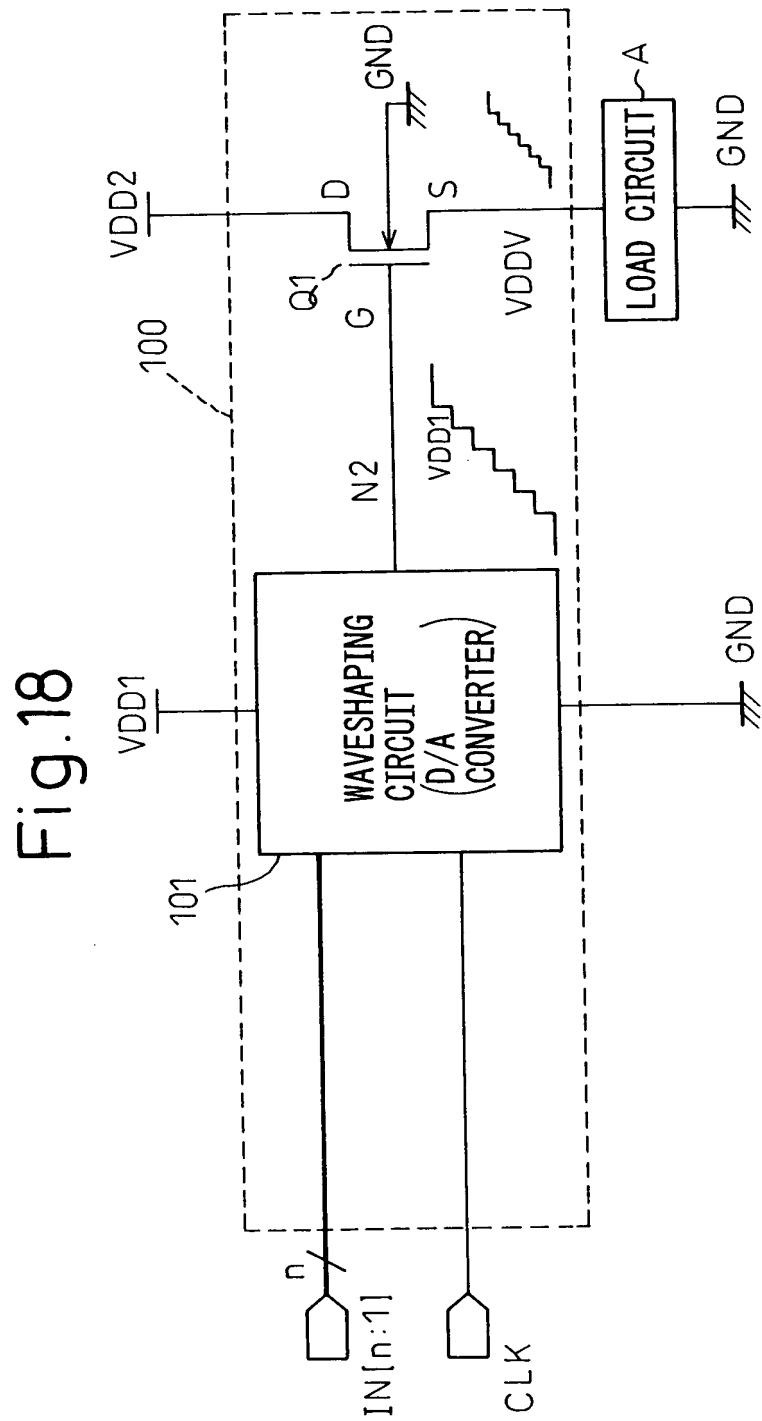
Inventor's Name: MIYAGI
Application No.: NEW
Docket No.: 100021-00133

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Fig.17

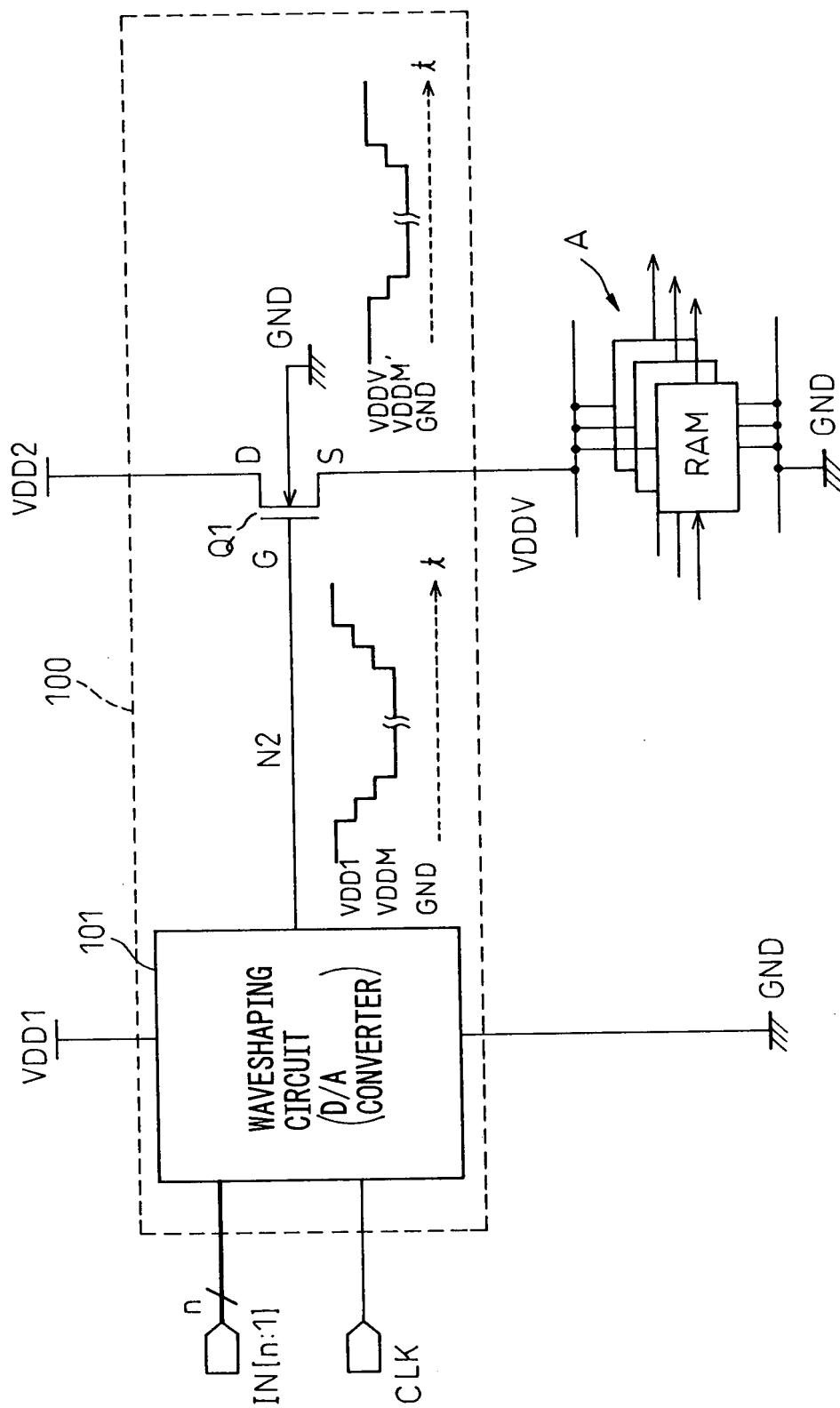


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Fig. 19



Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING A LEAKAGE CURRENT CUTOFF CIRCUIT, CONSTRUCTED USING MT-CMOS, FOR REDUCING STANDBY LEAKAGE CURRENT

REReducing STANDBY LE
Inventor's Name: MIYAGI
Application No.: NEW
Docket No.: 100021-00133

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Fig. 20

